In the Office Action, claims 13 and 17 were rejected under 35 USC 112, as being indefinite for failing to particularly point out and distinctly claim the subject matter claimed as invention.

Accordingly, please amend claims 13 (line 6 and line 10) by replacing "said first complementary transistor network" with --said transistor network--, and replacing "said first transistor network" with --said transistor network--. Also, please amend claim 17 by replacing "further comprises" with --performs the steps of--.

Rejection under 35 USC 102(b):

In the Office Action, claim 13 was rejected under 35 USC 102(b) as being anticipated by Miyashita *et al.* (IEEE, pp. 91-94, 1997).

The Applicant respectfully traverses these rejections based on the following reasons.

Firstly, Miyashita discloses a circuit for providing analog to digital conversion in applications requiring reduced power consumption, and minimized hysteresis. Contrarily, the present invention discloses a circuit employed in a receiver for receiving wireless transmission. This circuit as claimed in claim 13, performs fundamentally a two step operation, that includes, translating (shifting) the incoming wireless signal downward in frequency by a commutator network. Nowhere is this operation disclosed in Miyashita.

Secondly, the connectivity of the elements in the circuit of Fig. 3 of Miyashita is different than the connectivity of the elements in the present invention as claimed in claim 13. For example, Miyashita does not show an operational amplifier in a non-inverting unity follower configuration.

Thirdly, the level shifter in Fig. 3 (which is the transistor network of Fig. 4) in Miyashita has a current input. This is due to the presence of the V-I converter preceding the level shifter. Contrarily, in the present invention, the transistor network has a voltage input (claim 13, lines 4-8).

Clearly, the cited reference differs substantially from the present invention. Accordingly, the rejections of claim 13 should be withdrawn.

Furthermore, during the interview the Examiner expressed the opinion that claim 13 was a separate invention from the other claims and further stated that a restriction would be required. In order to expedite issuance of the other claims, Applicant authorizes the Examiner to cancel claim 13 by Examiner's amendment upon allowance of the remaining claims, reserving the right to pursue the invention of claim 13 with a continuing application.

Rejection under 35 USC 103(a):

In the Office Action, claims 1-8, 10-12, 14-19, were rejected under 35 USC 103(a) over Kotowski *et al.*(US. No. 5,561,660).

The Applicant respectfully traverses these rejections based on the following reasons, and considering the amendments which have been made to the claims.

The Examiner may be correct that the negative unity gain amplifier 41 and the switches 43 and 45 of Kotowoski together can be considered as an inverter commutator. However, if this assumption is made, it must take into account the intended purpose of the Kotowski reference, that being to provide offset and phase correction in delta-sigma modulators (Col 3, lines 8-9) utilizing a switching technique during different sampling periods to eliminate the effect of DC offsets (Col 3, lines 12-14).

Kotowski teaches (Col 6, lines 18-58) that when switches 43 and 49 are closed during one half period of the inverter clock, the output bit stream of the offset and phase correction delta-sigma modulator 20 represents an analog input signal: 01 = A * V1 + Voff and during the opposite half period of the inversion clock when switches 45 and 51 are closed, the output bit stream of the offset and phase correction delta sigma modulator represent a second analog input signal 02 = A * V1 - Voff. Kotowski concludes that by summing N values of 01 and N values of 02 that contribution of DC offset (Voff) is eliminated (Col 6, lines 52-60).

The Kotowski reference further teaches that for the offset and phase correction delta-sigma modulator to operate, the input signal 22 must be a baseband signal that includes zero frequency and that the inverter clock rate must be much less than the conversion clock rate in order to facilitate measurement of 01 and 02 to within an acceptable error (Col 5, lines 35-40).

The switches 43, 45, 49 and 51 (Kotowski Fig.3) clearly can not be operated at the same clock rate having a predetermined frequency as the delta-sigma modulator, as now required by the amended claims. This is because the inverter clock rate is less than the conversion clock rate in order to facilitate measurement of 01 and 02 to within an acceptable error. Thus, in summary, if the switches are operated at the same frequency, the circuit in Kotowski would not serve any useful purpose, or make sense, as it would be equivalent to averaging a single number.

The Examiner, during the interview, accepted the Applicant's argument, and suggested amending claims 1, 7, and 14 to differentiate the present invention from the Kotowski reference to make the claims allowable. The Examiner specifically suggested or concurred in the addition of the phrase, --having a predetermined frequency-- in the first feature of the claims, and further adding --operating at said predetermined frequency-- in the second feature of the claims. The Examiner also recommended amending the preamble of claim 7, by including the phrase --circuit employed in a--. Accordingly, the Applicant has amended claims 1, 7, and 14 to make them allowable. Dependent claims 2-6, 8, 10-12, and 15-19 depend on the amended independent claims and are now in condition for allowance.

Accordingly, it is respectfully suggested that the application is in condition for allowance, and issuance of the Notice of Allowance at an early date is in order. In the event that the application is not now entirely in condition for allowance, it would be appreciated if the Examiner would telephone the undersigned.

Thank You.

Respectfully submitted,

Date: June 13, 2001

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